IN THE CLAIMS:

1. (Original) An application specific integrated circuit, comprising:

a programmable logic core having an array of dynamically configurable arithmetic logic units;

a network interface subsystem, including a media access controller, configured to employ a first portion of the programmable logic core that interfaces with the media access controller and that is configurable to process control data; and

a data transmission subsystem associated with a memory device and configured to employ a second portion of the programmable logic core that stores received data from the network interface subsystem to the memory device and sends transmission data from the memory device to the network interface subsystem in response to an instruction from a host system.

2. (Previously Presented) The application specific integrated circuit as recited in Claim 1 wherein the first portion and the second portion are embodied within a plurality of programmable logic cores.

3. (Original) The application specific integrated circuit as recited in Claim 1 wherein the programmable logic core is configurable to dynamically implement functions based on information received from the host system.

4. (Original) The application specific integrated circuit as recited in Claim 3 wherein the programmable logic core is configurable to program new functions while executing

previously implemented functions.

5. (Original) The application specific integrated circuit as recited in Claim 1 wherein the programmable logic core is coupled to the host system by a slave bus, the programmable logic core further configured to be a slave device.

6. (Previously Presented) The application specific integrated circuit as recited in Claim 5 further including an adapter subsystem, and a data bus interface subsystem that couples the adapter subsystem and the programmable logic core to the slave bus.

7. (Original) The application specific integrated circuit as recited in Claim 6 wherein the adapter subsystem includes a programmable logic core test circuit, a parallel interface subsystem that couples the adapter subsystem to the data bus interface subsystem, and a serial programming interface subsystem.

8. (Original) The application specific integrated circuit as recited in Claim 6 further including a control/test interface bus that couples the adapter subsystem to the programmable logic core.

9. (Original) The application specific integrated circuit as recited in Claim 1 wherein the programmable logic core is further coupled to the host system by a master bus, the programmable logic core further configured to be a master device to independently control the

master bus.

10. (Original) The application specific integrated circuit as recited in Claim 1 wherein the first portion is configured to process control data and the second portion is configured as a direct memory access controller.

11. (Original) The application specific integrated circuit as recited in Claim 1 wherein the first portion is couplable to the host system by a control bus and the second portion is couplable to the host system by a data bus.

12. (Original) The application specific integrated circuit as recited in Claim 1 wherein the first portion is configured to include a control register, a statistics counter and a media independent interface manager.

13. (Original) The application specific integrated circuit as recited in Claim 1 further including first-in-first-out buffers coupled to the network interface subsystem and the data transmission subsystem, one of the first-in-first-out buffers configured to buffer data received from the network interface subsystem and another of the first-in-first-out buffers configured to buffer data received from the data transmission subsystem.

14. (Original) The application specific integrated circuit as recited in Claim 1 wherein the network interface subsystem is configured as an ethernet controller.

15. (Previously Presented) A method of operating an application specific integrated circuit, comprising:

dynamically configuring arithmetic logic units in a programmable logic core;

employing a first portion of the programmable logic core to process control data and interface with a media access controller of a network interface subsystem; and

employing a second portion of the programmable logic core to store received data from the network interface subsystem to a memory device and to send transmission data from the memory device to the network interface subsystem in response to an instruction from a host system.

16. (Original) The method as recited in Claim 15 wherein employing the first portion and the second portion includes employing first and second portions embodied within a plurality of programmable logic cores.

17. (Original) The method as recited in Claim 15 wherein dynamically configuring the programmable logic core includes dynamically configuring the programmable logic core to dynamically implement functions based on information received from the host system.

18. (Original) The method as recited in Claim 17 wherein dynamically configuring includes programing the programmable logic core with new functions while the programmable logic core executes previously implemented functions.

19. (Original) The method as recited in Claim 15 further including providing a connection between the programmable logic core and the host system by a slave bus and configuring the programmable logic core to be a slave device.

20. (Previously Presented) The method as recited in Claim 19 further including an adapter subsystem, and a data bus interface subsystem that couples the adapter subsystem and the programmable logic core to the slave bus.

21. (Previously Presented) The method as recited in Claim 20 wherein the adapter subsystem includes a programmable logic core test circuit, a parallel interface subsystem that couples a support logic core to the data bus interface subsystem, and a serial programming interface subsystem.

22. (Original) The method as recited in Claim 20 further including a control/test interface bus that couples the adapter subsystem to the programmable logic core.

23. (Original) The method as recited in Claim 15 further including providing a connection between the programmable logic core and the host system by a master bus, and configuring the programmable logic core to be a master device to independently control the master bus.

24. (Original) The method as recited in Claim 15 wherein dynamically configuring

includes configuring the first portion to process control data and configuring the second portion as a direct memory access controller.

25. (Original) The method as recited in Claim 15 further including providing a connection between the first portion and the host system by a control bus and providing a connection between the second portion and the host system by a data bus.

26. (Original) The method as recited in Claim 15 wherein dynamically configuring includes configuring the first portion to include a control register, a statistics counter and a media independent interface manager.

27. (Original) The method as recited in Claim 15 further includes buffering data received from the network interface subsystem in a first-in-first-out buffer and buffering data received from the data transmission subsystem in a second first-in-first-out buffer.

28. (Original) The method as recited in Claim 15 wherein dynamically configuring includes configuring the first portion as an ethernet controller.

29. (Original) A network interface system, comprising:

a host system; and

an application specific integrated circuit, including:

a programmable logic core having an array of dynamically configurable arithmetic

logic units;

a network interface subsystem, including a media access controller, configured to employ a first portion of the programmable logic core that interfaces with the media access controller and that is configurable to process control data; and

a data transmission subsystem associated with a memory device and configured to employ a second portion of the programmable logic core that stores received data from the network interface subsystem to the memory device and sends transmission data from the memory device to the network interface subsystem in response to an instruction from the host system.

30. (Previously Presented) The network interface system as recited in Claim 29 wherein the first portion and the second portion are embodied within a plurality of programmable logic cores.

31. (Original) The network interface system as recited in Claim 29 wherein the programmable logic core is configurable to dynamically implement functions based on information received from the host system.

32. (Original) The network interface system as recited in Claim 31 wherein the programmable logic core is configurable to program new functions while executing previously implemented functions.

33. (Original) The network interface system as recited in Claim 29 wherein the

programmable logic core is coupled to the host system by a slave bus, the programmable logic core further configured to be a slave device.

34. (Previously Presented) The network interface system as recited in Claim 33 further including an adapter subsystem, and a data bus interface subsystem that couples the adapter subsystem and the programmable logic core to the slave bus.

35. (Previously Presented) The network interface system as recited in Claim 34 wherein the adapter subsystem includes a programmable logic core test circuit, a parallel interface subsystem that couples a support logic core to the data bus interface subsystem, and a serial programming interface subsystem.

36. (Original) The network interface system as recited in Claim 34 further including a control/test interface bus that couples the adapter subsystem to the programmable logic core.

37. (Original) The network interface system as recited in Claim 29 wherein the programmable logic core is further coupled to the host system by a master bus, the programmable logic core further configured to be a master device to independently control the master bus.

38. (Original) The network interface system as recited in Claim 29 wherein the first portion is configured to process control data and the second portion is as a direct memory access controller.

39. (Original) The network interface system as recited in Claim 29 wherein the first portion is couplable to the host system by a control bus and the second portion is couplable to the host system by a data bus.

40. (Original) The network interface system as recited in Claim 29 wherein the first portion is configured to include a control register, a statistics counter and a media independent interface manager.

41. (Original) The network interface system as recited in Claim 29 further including first-in-first-out buffers coupled to the network interface subsystem and the data transmission subsystem, one of the first-in-first-out buffers configured to buffer data received from the network interface subsystem and another of the first-in-first-out buffers configured to buffer data received from the data transmission subsystem.

42. (Original) The network interface system as recited in Claim 29 wherein the network interface subsystem is configured as an ethernet controller.